IC Package and Bonding Wire Modeling Software and Its Application to RFIC Design

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Abstract — **This paper presents an IC package and bonding wire modeling software which generates an equivalent lumped circuit model from physical information of IC package and bonding wires. The resulting model takes into account the effects of frequency-dependent resistance, capacitance, as well as self and mutual inductance. The accuracy of the modeling approach has been verified using a 20-pin lead-less plastic chip carrier package. Furthermore, the application of the IC package characterization software to the design of a 700 MHz CMOS VCO has also been demonstrated.**

I. INTRODUCTION

An accurate model of an IC package, which consists of leadframe and bonding wire models, is an important feature in successful high-frequency circuit design [1, 2]. This is because at high-frequencies parasitic elements such as self and mutual inductance can have significant effect on circuit performance [1, 2]. Furthermore, in the course of high-frequency design, pin assignment, die size, and die position can often change, which in turn requires frequent changes in bonding wire model.

Often, equivalent circuit models of packages are obtained from S-parameters of E&M simulations [3, 4] or direct measurements [5, 6]. E&M simulations involve three-dimensional numerical computation, and hence their inherent disadvantage is a long simulation time. Similarly, package measurements, especially of large packages are difficult due to a large number of pins. Therefore, there is a need for a more efficient package characterization approach where an accurate equivalent circuit model of the package can be generated.

In this paper, an IC package and bonding wire modeling software is presented. The software is based on analytical techniques developed by Grover [7] in order to achieve short simulation time. The output of the characterization program is a SPICE subcircuit net-list. The modeling procedure and formulation are shown in Section II. Then, the experimental verification of the program is presented in Section III using S_{11} parameter measurements with a 20-pin lead-less plastic chip carrier (LPCC20) package. Moreover, the application of the package and bonding wire modeling software in a design of a 700 MHz CMOS VCO is also presented. The measurements of the VCO demonstrate the validity and usefulness of the software.

II. MODEL AND FORMULATION

The leadframe of a package and bonding wires are modeled separately. The models are derived from their geometrical information. Fig. 1(a) shows an example of the top view of a 4-pin package to explain the modeling process.

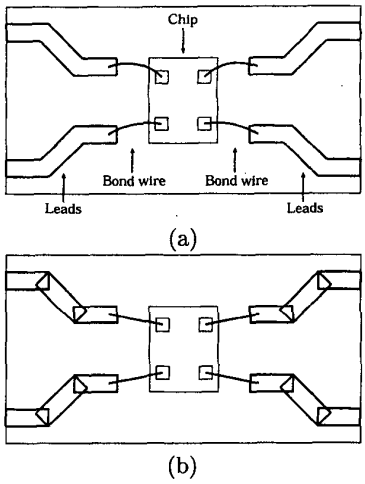

Figure 1: (a) An example of the package. (b) The leads and bonding wires are approximated by piece-wise linear sections.

At first, the shapes of leads of the leadframe and bonding wires are simplified as shown in Fig. 1(b). The leads are approximated with a series connection of piece-wise linear sections. On the other hand, the bonding wire is replaced with one straight section. Although the bonding wires bend vertically, the lengths are extracted from their top view. In order to take this bending into account, an empirical coefficient can be used, if necessary, to multiply the length. Each cross-section for the leads and bonding wires is assumed to have rectangular-pole and cylindrical shape, respectively.

Secondly, equivalent circuit models for each section for the leads and bond-wires, and mutual effects among all the sections are calculated. The equivalent circuits for the rectangular-pole-shaped sections such as leads are

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derived from their length, width and thickness, while those for cylindrical ones like bond-wires are from their length and radius. On the other hand, the mutual effects between two sections are estimated with a distance and an angle between them. Throughout these model calculations, physical constants of the sections and the package medium are also used. For example, resistivity, ρ, is used for dc and ac resistance extractions, and dielectric constant, ϵ, for mutual capacitances.

The equivalent circuit models for two sections including mutual components are shown in Fig. 2. As shown in the figure, the equivalent model for each section consists of a self-inductance, $L_{p,self}$, and a lumped model for the skin effect with $R_{p,i}$ and $L_{p,i}$ ($p = \{1, 2\}$ and $i < n$ is a positive integer). Here, the skin depth is considered for the ac resistance calculations. In addition, the user can choose the number of elements, n, for the RL sections and frequencies at which $L_{p,i}$ and $R_{p,i}$ are evaluated.

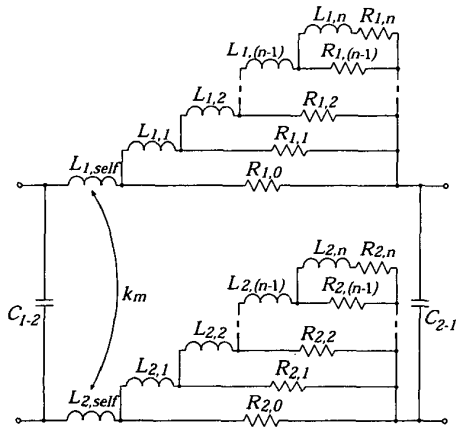


Figure 2: Equivalent circuit models for two sections.

The mutual components are the mutual inductance with coupling coefficient of k_m and the mutual capacitance whose effect is equally shared with two capacitances, C_{1-2} and C_{2-1}, as shown in the figure. The mutual elements between all the possible combinations of two arbitrary sections are independently estimated for each pair.

The self and mutual inductances are calculated using techniques developed by Grover [7]. On the other hand, a simple analytical technique is employed for a rapid estimation of the mutual capacitances instead of using a numerical computation. That is, self voltage coefficients of all the sections are calculated first. Then, the mutual voltage coefficients between arbitrary two of them are computed. Finally, the mutual capacitances are obtained from the coefficients.

After model parameter calculations, a SPICE subcircuit net-list that contains equivalent circuits for all the leads and bonding wires in it is produced.

III. Experimental Verification

The validity of the package model is demonstrated through measurements of an LPCC20 plastic package itself with a dummy chip and an integrated 700 MHz CMOS VCO in an LPCC20 plastic package.

A. S_{11} Measurements with Dummy Chip

A dummy chip which has two short connections at bonding pads are used. The chip is placed off-center as shown in Fig. 3 to make two different sets of bonding wire conditions. The measurements are done using Cascade Microtech FPC-GS probes [8] and Agilent HP4396B network analyzer with HP85046A S-parameter test set. The FPC-GS probes can directly contact the chip pins so that the use of special test fixtures and involved calibration procedures can be avoided. This ensures accurate S-parameter measurements.

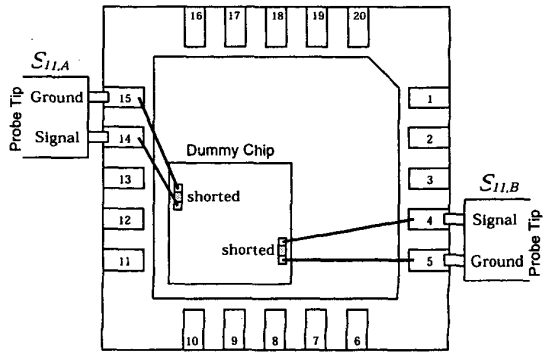
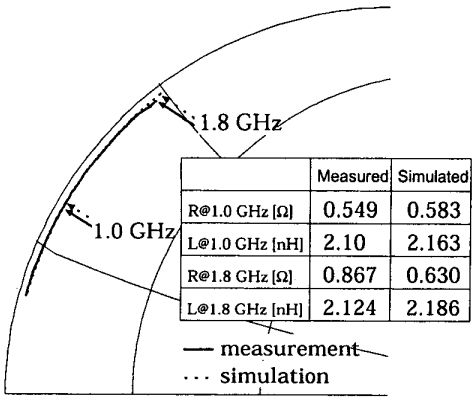


Figure 3: S_{11} measurements with a dummy chip and FPC probes.

S_{11} parameters are measured for two adjacent pins that are shorted on the dummy chip as shown in Fig. 3. Fig. 4 shows the measured results and SPICE simulation results using the package model. In the figure, a part of the Smith chart is shown for the inductance and resistance values at 1 GHz and 1.8 GHz summarized in a table. As shown in the figure, the SPICE simulations with the package model are in good agreements with the measurements.

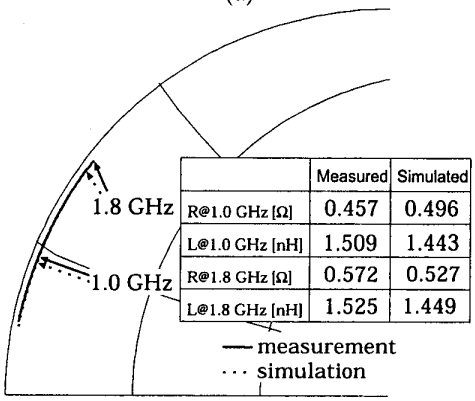
B. VCO Measurements

As an illustration of an actual IC design with the program, a VCO circuit has been designed and fabricated in a 0.35 μm CMOS process. The VCO has been packaged



	Measured	Simulated
R@1.0 GHz [Ω]	0.549	0.583
L@1.0 GHz [nH]	2.10	2.163
R@1.8 GHz [Ω]	0.867	0.630
L@1.8 GHz [nH]	2.124	2.186

(a)



	Measured	Simulated
R@1.0 GHz [Ω]	0.457	0.496
L@1.0 GHz [nH]	1.509	1.443
R@1.8 GHz [Ω]	0.572	0.527
L@1.8 GHz [nH]	1.525	1.449

(b)

Figure 4: Measured and simulated S_{11} parameters for (a) $S_{11,A}$, and (b) $S_{11,B}$ shown in Fig. 3.

in the LPCC20 plastic package that is mounted on an FR-4 circuit board with other components.

In the following simulations, the effects of the wire traces on the circuit board are also considered. The circuit board parasitics are extracted with the same technique as the package modeling proposed in this paper.

The circuit diagram of the VCO and the chip microphotograph are shown in Fig. 5 and Fig. 6, respectively. As shown in Fig. 5, the VCO is a standard LC oscillator with a cross-coupled differential pair as a negative conductance. Moreover, a differential buffer circuit is added to drive the external 50 ohm measurement equipment.

The LC tank circuit is placed off the chip. Because of the external tank arrangement, it is possible to examine the effects of the package parasitics to oscillation characteristics. For example, it is common to observe parasitic oscillations with the external LC tank VCO [2].

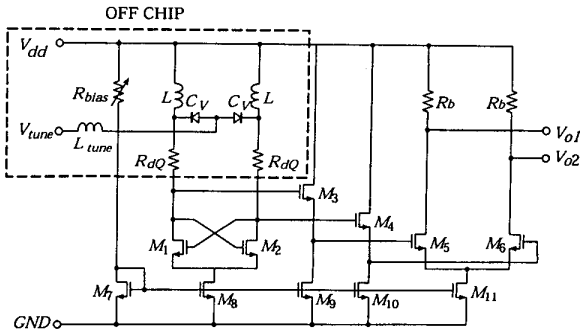


Figure 5: Schematic of the VCO.

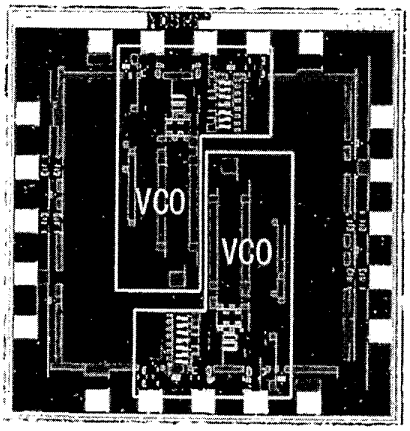


Figure 6: Microphotograph of the VCO chip. Two identical VCOs were integrated. Either one of them has been used for the measurements.

The Q-degradation resistors, R_{dQ}, in the figure are inserted to suppress the parasitic oscillations due to package parasitics. SPICE simulations with the package model obtained with the proposed program predict the parasitic oscillations without these resistors as shown in Fig. 7. From these results, the proper resistors for the desired frequency responses are determined. The final characteristics of the VCO designed with the package model are shown in Fig. 8.

The chip is tested using an HP4352B VCO/PLL analyzer. The measured response from the VCO is shown in Fig. 8. As shown in the figure, the voltage–frequency characteristics are in good agreements with SPICE simulations with the model. However, about 1.5 dB differences between measurements and simulations are observed in the output levels.

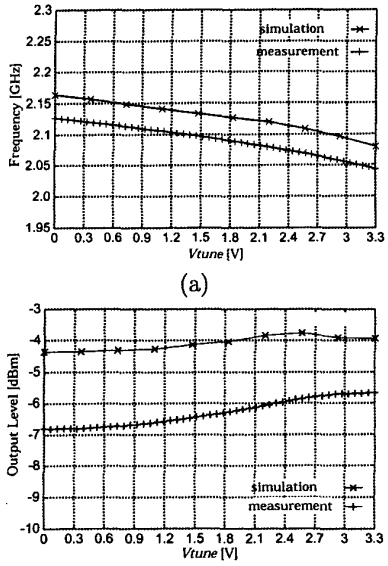


Figure 7: Simulated and measured results of the VCO without the degradation resistors, R_{dQ}. (a) Frequency characteristics, and (b) output level characteristics.

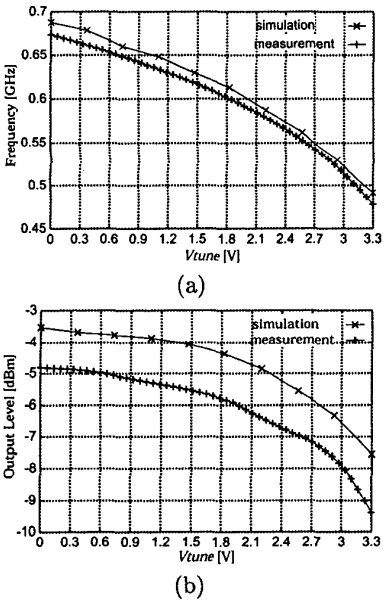


Figure 8: Simulation and measured results of the designed VCO. (a) Frequency characteristics, and (b) output level characteristics.

The parasitic oscillations are also observed by removing the Q-degradation resistors as shown in Fig. 7. Although the measured responses are not exactly predicted by simulations, the tendency of the tuning curves are well preserved. Nevertheless, this design example strongly suggest that the proposed package modeling program is useful for practical RFIC design process.

IV. CONCLUSIONS

An intuitive IC package modeling software that generates equivalent circuits of leads and bonding wires as SPICE subcircuits has been developed. The accuracy has been verified through LPCC20 plastic package measurements. As an application of the package modeling method, the CMOS VCO has been designed. Future works include accuracy improvements and graphic user interface (GUI) developments.

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